REMARKS

Claims 1-3, 5-13, and 15-66 are currently pending. Claims 1, 12, 15, 16, 30-42, 61, 63, and 65 are currently being amended, claim 4 is currently being cancelled, and claim 14 was previously canceled. Applicant reserves the right to pursue original and other claims in this and in other applications.

Claims 15 and 16 stand objected to because they depend from a canceled claim. The claims have been amended to correct their respective dependency, therefore the objection of these claims should be with drawn and the claims allowed.

Claims 1-5, 7-13, 17-18, 22-25, 27-29, 42, and 46-48 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Towler et al. (U.S. 6,618,279) ("Towler"). This rejection is respectfully traversed.

Claim 1 recites, *inter alia,* a test circuit for testing a match detection circuit, said test circuit comprising "a test line for providing a load to the match detection circuit; and a switch for switchably coupling the test line to a first line of the match detection circuit to provide the load on the first line for testing whether the match detection circuit is correctly indicating either a match or mismatch."

Towler discloses "A method for determining a desired operating impedance for a computer memory circuit includes applying, to a reference circuit, a test impedance value to a reference circuit. The test impedance value is controlled by a binary count. A determination is made, based upon the applied test impedance value, whether the reference circuit is in either a first state or a second state. The binary count is incremented if the reference circuit is in the first state and decremented if the reference circuit is in the second state. A condition is determined in which the reference circuit oscillates between the first state and said second state, and a pair of binary count

values is stored. The desired operating impedance for the computer memory circuit corresponds to the lower of the stored pair of binary count values." (Towler, Abstract)

Towler fails to disclose or suggest "testing whether the match detection circuit is correctly indicating either a match or mismatch." In the claimed invention, the feature is the match detection circuit's ability to properly reflect a match or a mismatch that would occur during operation of the match detection circuit. Depending on the feature, the circuit is tested to determine its ability to hold a charge or be pulled to ground. The claimed invention is different from Towler which seeks to determine the operating impedance of a match detection circuit. As such, the claimed invention and the invention of Towler are different. Therefore, the rejection of claim 1 should be withdrawn and the claim allowed.

Claims 2-5 and 7-11 depend, directly or indirectly, from claim 1 and are allowable for at least the reason noted above with respect to claim 1.

Claims 12 and 24 have a similar limitation as claim 1 and are allowable for at least the reasons noted above with respect to claim 1.

Claims 13 and 17-18; and 25 and 27-29 depend, directly or indirectly, from claim 12 or 24, respectively, and are allowable for at least the reason noted above with respect to claim 1.

Claim 22 recites, *inter alia*, a test circuit for a match detection circuit, said test circuit comprising: "a test circuit for providing a first load to said match detection circuit to test a margin of said match detection circuit."

Towler fails to disclose testing a "margin of said match detection circuit." To contrary, Towler tests the operating impedance. As such, the claimed invention and the

invention of Towler are different. Therefore, the rejection of claim 22 should be withdrawn and the claim allowed.

Claims 23-25 and 27-29 depend, directly or indirectly, from claim 22 and are allowable for at least the reason noted above with respect to claim 22.

Claims 6, 15-16, 19-21, 26, 30-41, 43-45, and 49-66 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Towler et al. (U.S. 6,618,279) ("Towler"). This rejection is respectfully traversed.

Claims 6; 15-16 and 19-21; and 26 depend, directly or indirectly, from claims 1, 12, and 22 and are allowable for at least the reason noted above with respect to those claims.

Additionally, with respect to claims 6, Towler does not teach pull up resistance. Nor is there documentation provided or identified to support the Examiner's position that it would have been obvious to enhance Towler to achieve the claimed invention. As such, the rejection should be withdrawn and the claim allowed.

Additionally, with respect to claims 15-16, 19-21, 26, it not shown how the teachings of Towler would achieve the claimed invention. Nor is there documentation provided or identified to support the Examiner's position that it would have been obvious to enhance Towler to achieve the claimed invention. As such, the rejection should be withdrawn and the claims allowed.

With respect to claim 30, which recites, *inter alia*, a test circuit for testing a match detection circuit, said test circuit comprising: "a test circuit controller; a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines

comprises: a load, wherein said load is a resistor; and a test line transistor for switchably coupling said load and said matchline for testing whether the match detection circuit is correctly indicating either a match or mismatch, a gate of said test line transistor coupled to said test circuit controller."

Towler fails to disclose "said feature is the match detection circuit is correctly indicating either a match or mismatch." As such the rejection of claim 30 should be withdrawn.

Claims 31-42 have similar limitations as claim 30 and should be allowed for at least the same reason as claim 30.

Claims 43-45 depend, directly or indirectly, from claim 42 and are allowable for at least the reason noted above with respect to that claim.

Claim 49 recites, *inter alia*, a method of testing a match detection circuit, comprising the step of: "precharging a matchline of said match detection circuit; applying a load to said matchline to test a feature of the match detection circuit; comparing a stored bit in said match detection circuit with a comparand bit; and determining whether said matchline is pulled to ground when a mismatch occurs in said comparing step."

Towler fails to disclose "determining whether said matchline is pulled to ground when a mismatch occurs in said comparing step." As such, the rejection of claim 49 should be withdrawn and the claim allowed.

Claims 50-52 depend, directly or indirectly, from claim 49 and are allowable for at least the reason noted above with respect to that claim.

Claim 57 has a similar limitation as claim 49 and should be allowable for at least the reason noted above.

Claims 58-60 depend, directly or indirectly, from claim 57 and are allowable for at least the reason noted above with respect to that claim.

Claim 53 recites, *inter alia*, a method of testing a match detection circuit, comprising the step of: "precharging a matchline of said match detection circuit; applying a load to said matchline to test a feature of the match detection circuit; comparing a stored bit in said match detection circuit with a comparand bit; and determining whether said matchline is pulled to ground when a match occurs in said comparing step."

Towler fails to disclose "determining whether said matchline is pulled to ground when a match occurs in said comparing step." As such, the rejection of claim 53 should be withdrawn and the claim allowed.

Claims 54-56 depend, directly or indirectly, from claim 53 and are allowable for at least the reason noted above with respect to that claim.

Claim 61 recites, *inter alia*, a content addressable memory, comprising: "a match detection circuit coupled to a match line and a discharge line; and a test circuit for testing said match detection circuit, said test circuit comprising: at least one test line for testing a feature of said match detection circuit, wherein said test line comprises: a resistance; and a test line transistor for selectively coupling said resistance between said matchline and a voltage source line for testing whether the match detection circuit is correctly indicating either a match or mismatch."

Towler fails to disclose "for testing whether the match detection circuit is correctly indicating either a match or mismatch." As such, the rejection of the claim should be withdrawn and the claim allowed.

Claims 63 and 65 have a similar limitation as claim 61 and should be allowable for at least the reason noted above.

Claims 62, 64, and 66 depend, directly or indirectly, from claims 61, 63, and 65, respectively, and are allowable for at least the reason noted above with respect to those claims.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: December 26, 2006

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Michael A. Weinstein
Registration No.: 53,754
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant